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This design guide is presented by Micro-Hybrid Dimensions, Inc. for the purpose of providing basic design information to our customers. Throughout the Design Guide Micro Hybrid Dimensions, Inc. will be referenced as MHD.

For quick reference a 4 page set of condensed design guidelines and capabilities is furnished at the start of this manual. Following these condensed guidelines is the detailed manual.

MHD is a long standing member of IMAPS, and some of the information presented has been adapted from the IMAPS Design Manual.

MHD has made every effort to have this information as accurate as possible. However, no responsibility is assumed by Micro Hybrid Dimensions for its use nor for any infringements of rights of third parties which may result from its use. MHD reserves the right to revise the content without prior notice.


Ted Myers
Dave Michal


*WE TAKE THE EXTRA STEPS*

This condensed version of thick film design guidelines is presented as a quick reference for hybrid circuit layout decisions. A more detailed 115-page design manual is also available as a courtesy of Micro-Hybrid Dimensions. The manual details all aspects of thick film design, layout and inspection. It may be obtained be contacting:

# Table of Contents

# Definition of Thick Film and the Manufacturing Process

Screen Printing is the transfer of thixotropic pastes (pastes that the viscosity decreases with increasing shear rates), through a fabric screen onto a substrate. This transfer occurs when the paste comes in contact with the substrate surface and in pulled through the screen. The high shear action of the squeegee passing over the screen allows this transfer to occur. The paste is deposited in a pattern defined by the open areas in the emulsion of the screen.

The term thick film has gained acceptance as the preferred generic description for that field of microelectronics in which specially formulated pastes are applied and fired onto a ceramic substrate in a definite pattern and sequence to produce a set of individual components, such as resistors and capacitors, or a complete functional circuit. The types of pastes employed belong to three basic groups: conductive, dielectric and resistive and are applied using stainless steel screens. High-temperature firing matures the thick film elements and bonds them integrally to the ceramic substrate. After firing, the typical thickness of a thick film element will be 0.4 to 1 mil or more.

Single layer circuits contain one layer of conductive material. Resistor arrays are also single layer circuits, strictly speaking, but consist only of one conductive and one or more resistive layers.

Multilayer circuits consist of two or more conductive layers separated by dielectric layers to prevent electrical shorts between them. Deliberate contacts between different conductive layers are obtained through vias, i.e., openings in a dielectric layer (between two otherwise separated conductive layers) which are filled with conductive paste (via-fill) that provides electrical continuity between the two conductive layers. Multilayer circuits may also contain resistive layers. While resistors are generally printed directly on the substrate, they can also be printed on the top dielectric layer.

Artwork is typically created using commercially available Computer Aided Design (CAD) systems and then converted into Gerber format for photo plotting and 1X artwork generation. For multi-up arrays, stepping can be done either in the CAD system or from the Gerber file.

# Condensed Thick Film Hybrid Design Information

## CAPABILITIES

| Dimensional Constraints | | Min. (Inches) | Nominal (Inches) | |
|---|---|---|---|---|
| Conductor to Conductor Spacing - Same Layer | | | | |
| | Standard | 0.005 | 0.010 | |
| | Special | 0.004 | - | |
| Conductor Widths - | Standard | 0.005 | 0.010 | |
| | Special | 0.004 | - | |
| Conductor to Edge of Substrate | | 0.005 | 0.010 | |
| Wire Bonding Pad (Width / Length) | | 0.010 | - | |
| Conductor to Resistor Spacing | | 0.008 | 0.015 | |
| Upper & Lower Conductor to Connecting Conductor Overlap Length | | 0.005 | 0.012 | |
| Upper & Lower Conductor Width at Crossover | | 0.008 | 0.015 | |
| Dielectric to Resistor (Active Part) Spacing | | 0.010 | >0.030 | |
| Via and Corresponding Via Fill Spacing | | 0.008 | 0.012 | |
| Via to Adjacent Via Spacing Edge to Edge | | 0.010 | 0.015 | |
| Via to Adjacent Conductor Spacing | | 0.008 | 0.010 | |
| Via to Edge of Dielectric Spacing | | 0.015 | - | |
| Via to Edge of Substrate Spacing | | 0.025 | - | |
| Via to Via Spacing for Step Configuration | | 0.005 | 0.010 | |
| Via Hole Diameter - in Ceramic | | 0.006 | 0.008 | 0.015 Max. |
| Via Hole Diameter - in Dielectric | | 0.008 | 0.012 | |
| Via Hole Annulus (for via in ceramic) | | 0.005 | - | |

# Condensed Design Guidelines

1. On parts with metalized pads around non-plated-through holes, place a clear pad 0.005" larger than hole diameter over hole in metal layer of the gerber file.

2. Make sure the solder mask extends 0.005" beyond edge of feature. it is intended to cover.

3. If possible, design all resistors to be printed with the same paste (i.e. on the same layer) to have their current flow in the same direction - e.g. parallel to x-axis or y-axis of substrate.

4. For resistors of 50 Ohms and below specify probe points to allow for metalization resistance.

5. For best economics, specify 0.008" via in ceramic, covered with solder mask for side-to-side continuity rather than wrap around edges.

6. For best economics, specify parts to be shipped in full array form rather than strips or singles

7. Put part number and artwork revisions on each layer of gerber files.

8. If text is to be printed in solder mask or metal, ensure minimum font line width of 0.007" for printability.

9. Avoid openings in printed features of less than 0.015" dia., and Square corners.

10. Keep trace widths $\geq$ 0.010" of possible for best economics.

11. For Best economics design array parts to fit on 4.00" X 4.00" printed area using 0.025" thick unannealed 96% Alumina.

12. Avoid metalization crossing snap lines if possible. Keep traces and printed features 0.010" from snap lines.

13 Keep solder mask minimum 0.005" away from features to be kept free of solder mask. E.G., windows for solder pads should be 0.010" larger than minimum exposed solder pad to allow paste spreading alignment and screen distortion.

# MHD Customer Capabilities

- Fast Turnaround on Prototypes
- Design Recommendations
- CAD Design From Boards and Schematics
- Extensive R & D Expertise With Hybrids
- Competitive Pricing
- Quality to Commercial, Military, and Medical Standards
- Flip Chip Mounting
- Surface Mounting Technology
- Chip on Board, Chip & Wire
- Full Service Substrates thru Assembly

*We Take The Extra Steps*

# MHD Thick Film Capabilities

| | |
|---|---|
| Line Dimensions: | 5 mil standard, As low as 4 mil available<br>For a dimensional guideline, see Micro-Hybrid Dimensions, Inc. Design Manual beginning with Table A. |
| Conductors: | Gold, Platinum Gold, Platinum Palladium Gold, Platinum Silver, Platinum Palladium Silver, Silver. |
| Substrates: | Alumina, Aluminum Nitride, Beryllia in thicknesses of 10, 15, 20, 25, 30, 40 and 60 mils, Stainless Steel up to 8” square printed area. |
| Resistor Values: | 0.10 ohms/square to 100 Meg ohms/square, over multilayers. |
| Resistor Trim: | 0.5% tolerance. |
| TCR: | Down to 50 PPM / °C. |
| Features: | Multilayers (up to 6 conductor layers)<br>Silver or gold through holes<br><br>Vias and via fills<br>Weldable, solderable and wire bondable conductors<br>Wraparounds (Edge Arounds)<br><br>DuPont, ESL, Heraeus, Metech principal pastes;<br>Others are available<br>Ni and solder plating over Thick Film<br>Resistors may be on top layer of multilayer<br>Thermistors<br>Thick film strain gage resistors<br>Surface mount available |
| Inspection: | Visual to MIL-STD-883 Method 2032 plus customer tests and requirements. |

# Types of Ceramics and Selections

The thick film industry has generally standardized on as-fired 96% Alumina, $Al_20_3$. Although other ceramics such as Beryllia and aluminum nitride can be and are used, most applications are 96% alumina. This material is both reasonably priced and compatible with resistor, conductor and dielectric pastes commonly used for thick film circuits.

Most product is furnished on a 25 mil substrate due to cost. For single layer circuits as large as 4.5 inches square, a 25 mil substrate is acceptable when specified at 0.003" per inch flatness. 0.002" per inch flatness can be ordered with price considerations.

A potential problem with deposited resistors exists when they are printed on a warped substrate and then the substrate is flattened in a mounting operation. The resistors are mechanically stressed and exhibit a change in resistance. The effect worsens as the resistor length or substrate length increases. Using a thicker substrate (40 mils or more) is one way to overcome this problem.

Special consideration must be given for multilayer substrates. Substrate warpage can occur as the dielectric thickness increases during circuit fabrication. The degree of warpage is a function of several factors: material coefficient of expansions, moduli of elasticity, material thicknesses, substrate length, etc. Some dielectric materials are better than others with respect to warpage characteristics. Therefore, each application should be examined individually and substrate thickness selected accordingly.

# Types of Materials

There are a large number of materials from many manufacturers in each composition class, and specific detailed information can be obtained from MHD. The proper selection is based on the application and its particular requirements in the circuit.

## Conductors

### Silver Compositions

As a class, silver alloy conductor compositions are the most economical of the thick film conductor compositions. These conductors show the best initial adhesion of any of the conductor classes. They show good solderability and moderate to good solder leach resistance. Low palladium content silver conductors generally show the best compatibility when co-fired with ruthenium based resistor compositions. Silver alloy conductors generally have good gold wire bonding capability but are not recommended for aluminum wire bonding without thermal aging qualification tests. Hard solder die bonding is not possible with silver alloy conductors since it requires the formation of an AuSi eutectic. However, other solder alloy compositions can be compatible. The soldered adhesion to these conductors varies with the alloy and should be examined before selection. Likewise, the sheet resistance varies from less than two to 60 milliohms/square/half mil thickness and should be selected for specific circuit requirements.

Silver based conductors are susceptible to both solder leaching and migration under the combination of voltages and humidity / moisture conditions. In general these effects decrease with increasing percentages of Pd and Pt in the compositions.

### Palladium Gold Conductor Compositions

As a whole, this class of compositions provides greater ease of soldering with low tin solders and lower loss of adhesion on thermal aging with high tin solder than silver alloy conductor compositions. In addition, these compositions give better solder leach resistance when used with eutectic solder containing no silver. These conductors cannot generally be readily soldered when used as the top conductor over a crossover dielectric composition. PdAu compositions, as a class, show good gold wire bonding capability and can be hard solder die bonded under suitable conditions. Sheet resistance varies from 25-35 milliohms/square/half mil thickness.

### Platinum Gold Conductor Compositions

This class of thick film conductors is typically the most expensive per unit area printed, but gives the best leach resistance for thick film conductor compositions. These conductors are recommended especially in circuits where discrete components are attached with solder and where certain components must be replaced frequently because of the complexity of the circuit.

The compositions are suitable for gold wire bonding or die bonding. However, in die bonding, less flow out of the AuSi eutectic is experienced than with the gold compositions. Sheet resistance varies with the alloy, but is typically less than 100 milliohms/square/half mil thickness.

### Gold Conductor Compositions

Gold conductor compositions are preferred for both gold wire bonding and eutectic (AuSi and AuSn) die bonding. When eutectic (hard solder) attachments are made to conductors a more profuse flow out of the eutectic is obtained and permits convenient visual inspection. Gold wire bondability, although, metallurgically compatible, will vary with the gold composition and process history. Similarly, film adhesion to the ceramic or underlying dielectric can vary with the same parameters. Generally, the bondability of gold will decrease with repeated firing. Therefore, consideration should be given during the layer sequence design to minimize the number of subsequent firings.

For Aluminum wire bonding to thick film metallization, there are only a few alloys of gold that are reliable at elevated storage temperatures for long periods of time. The general failure mode for aluminum wire to gold thick film is a significant increase in electrical resistance at the AuAl interface. Supplier and user data indicate that the gold-low palladium content alloy can prevent the occurrence of high resistance aluminum wire bonds to gold.

## Dielectric

In thick film technology, dielectric materials have three principal uses:

- Capacitors
- Crossovers, multilayers and solder dams
- Encapsulation and hermetic seals

Thick film capacitors consist of a screened dielectric layer between two printed conductors. This permits the construction of capacitive devices on ceramic substrates. Dielectric crossovers provide good isolation between top and bottom conductors and isolate layers of conductors in multilevel arrays. Encapsulating dielectric films minimize the effects of moisture and reducing atmospheres on resistors and capacitors, and protect these elements during such processing steps as trimming. Glass hermetic seals are used mostly in the DIP packaging industry. Solder dams are used in those circuits that require solder to be confined to specific areas. In most cases, the same material used for crossovers and multilayers can be used for solder dams. Thick film resistors are generally coated with a low temperature vitreous glass for post trim stability, and environmental resistance.

# Design and Layout

## Conductor and Conductor Pad

This section gives the nominal and minimum conductor widths and spaces for most hybrid designs.

Critical parameters to consider during design:

- Capacitance - produces coupling to ground and other conductors.
- Inductance - critical at frequencies above 500 MHz.
- Resistance - a function of aspect ratio and paste resistivity.
- Characteristic Impedance - a transmission line characteristic dependent upon the materials and geometry, which becomes critical at high frequencies in analog circuits and high speed digital circuits.

Detailed analysis of conductor geometry's and the resulting electrical characteristics should be performed by the Project Engineer to insure adequate control of the above parameters to meet circuit performance specifications. The following guidelines are provided for specific requirements.

- The layout of thick-film conductors should conform to the requirements contained in Table A and Figure 1. Both minimum and preferred design dimensions are provided. The preferred design dimensions are recommended and represent the most economical approach based on production methods; however conductors should not be overly wide just to fill the substrate as conductor material is expensive.
- Conductors should be routed parallel to the substrate sides i.e., in the "X" or "Y" axis. Diagonal routing should not be utilized. For economy, the geometry of a pattern feature should be no more complex than is absolutely necessary. Whenever possible, create the thick film design using basic geometric forms such as squares, circles, lines, etc. to facilitate artwork creation.
- Conductors should be kept as short and wide as possible to minimize added circuit resistance, stray capacitance, and thermal coefficient of resistance (TCR) effects, particularly when terminating low-value resistors and for ground or transistor collector paths.
- Use an emergence pattern around the periphery of a component whenever possible to a provide standardized bonding display and aid assembly and inspection. See the Multilayer Design section and the section on Wire Considerations for additional information.
- Conductors should be routed around the attach pads of chip capacitors or other surface mount components. If absolutely necessary, route it between the pads and conductors using a minimum of 20 mils clearance between it and the capacitor to attach pads. In addition, coat it with dielectric or glass in the area beneath the components.
- If possible, for economic reasons use only one side of the substrate for circuitry. If not, other options for interconnecting the two sides include: edge arounds, soldered edge clips and metallized through holes.
- Wire termination bond pads should be as large as design will permit.
- Make sure any thick film resistor or capacitor have probe pads for trimming. Also include probe pads for any other continuity features to be tested , such as through holes of via testing. Minimum and preferred dimensions are specified in the guidelines shown in Table A.

TABLE A
DIMENSIONAL CONSTRAINTS FOR THICK FILM CONDUCTORS AND PADS
(See also Table B for Component Mounting)

| Conductor and Pad Sizes and Spacing | Minimum Dimension (Inch) | Nominal Dimension (Inch) | See Figures 1 & 2 |
|---|---|---|---|
| Conductor to edge of substrate | .005 | .010 | 1 |
| Exit bonding pads (width and length) | .015 x .020 | | 2 |
| Wire bonding pads (width and length) for one or two wires on same pad | .005 | .010 | 3 |
| Conductor Width (power and ground) | .010 | .015* | 4 |
| (signal) | .005 | .010 | |
| (special) | .003 | | |
| Conductor-to-Conductor Spacing | .010 | .015 | |
| (power to ground) | .005 | .010* | 5 |
| (signal to power and ground) | .005 | .010 | |
| (signal to signal) | .005 | .010 | |
| (special) | .003 | .010 | |
| Conductor-to-Resistor Spacing (on untrimmed side of resistor) | .010 | .015 | 6 |
| Conductor-to-Resistor Spacing (on trimmed side of resistor | .010 | .015 | 7 |
| Conductor-to-Resistor Spacing, top hat configuration (trimmed side of resistor) | .010 | .015 | 8 |
| Upper & Lower Conductor Width at Crossover Junction | .005 | .010 | 9 |
| Crossover Conductor-to-Connecting Conductor Overlap Length | .005 | .0125 | 10 |
| Conductor Crossover Dielectric Overlap | .005 | .015 | 11 |
| Printed Wire | .0025 | .015 | |
| Dielectric to Resistor (active part) Spacing | .010 | .020 | 12 |
| Wire Bond Clearance at Crossover | .015 | .020 | 13 |
| Wire Bond Clearance at Resistor | .015 | .020 | 14 |
| Probe Areas (sq.) | .015 | .020 | 15 |

*Dimension will also depend upon power and other circuit requirements.

Insert Figure 1

Insert Figure 2

# Mounting Pads Design and Layouts

Table B and Figure 3 give both minimum and preferred dimensions for device mounting pads. The following guidelines also apply:

- Metallized mounting pads should be provided for all chip devices. As a minimum, a metallized or glass ring should be provided to locate components attached with non-conductive epoxy.

- In design layout components should be depicted at maximum dimensions, increased to the next higher .005 inch increment. Use the largest component outline if there is more than one option for any given element.

- Layouts for artwork of epoxy or solder paste screens should have a dimensioned range from the rounded size to maximum of .005 inch larger on each side. Epoxy or solder paste prints should be a maximum size where possible but should not be closer than .010 to any interface such as wirebonds, adjacent pads or circuit lines.

- Mounting pads must be increased in size for those devices that specify mounting on molytabs. Molytab dimensions are at least .005"/side larger than the device dimensions. For proper mounting pad design, an additional .005"/side is needed for device bonding. Therefore, minimum and preferred dimensions are specified in Figure 3.

- Capacitor and resistor chips with wraparound end contacts should be oriented on the substrate to give the largest attachment area. They should not be oriented on edge or on end. The mounting pads for these devices must accommodate dimensional tolerances for chip components. Requirements for these pad dimensions are specified in Figure 4 and as follows:

    - Dimension A is a minimum distance of .010 inch.
    - Area B is for either epoxy or solder paste application.
    - Beads of non-conductive epoxy are typically added to the device sides when L is 200" or larger.
    - Dielectric solder dams should be used to contain excessive flow of solder in the attachment area. It is important that the areas bounded by the solders dams be equal at each end of the device. This ensures an equal amount of solder at each end of the device and facilitates self alignment during reflow.

- The width “W” of pads used for attachment of leaded devices should be three times the lead diameter/foot width or .050 inch, whichever is larger. The pad length is determined by the type of component to be mounted. Dielectric solder dams apply here also as in any solder-mounted component.

TABLE B
DEVICE MOUNTING PADS AND SPACINGS
(For Thick and Thin Film)

| Pad Sizing and Spacing | Minimum Dimension (Inch) | Nominal Dimension (Inch) | See Figure 3 |
|---|---|---|---|
| IC Semiconductor Chip-to-Chip Spacing | .025 | .050 | 1 |
| Active and Passive Chip or Molytab Mounting Pad excluding capacitors (width & length beyond chip) | .005 | .010 | 2 |
| Passive Chip-to-Bonding Pad Wiring Distance beyond chip (width or length) | 1/3 height +.005 | See * | 3 |
| Passive Chip Spacing-to-Wire Bonding Pad | 1/3 height +.005 | See * | 4 |
| Inductor Lead Mounting Pad (width and length) | .040 | .050 | 5 |
| Inductor Body-to-Lead Mounting Pad | .005 | .0075 | 6 |
| Passive Chip End-to-End Spacing | .020 | .030 | 7 |
| Chip Mounting Pad to Substrate Edge (adjacent to non-functional package lead or sidewall with no leads) | .025 | None | 8 |
| Inductor or Transformer Pad to Substrate Edge | .100 | None | 9 |
| Inductor or Transformer Pad to Adjacent Chip Pad | .030 | .050 | 10 |

* Maximum dimensions are in accordance with wire requirements.

# Crossover Design and Layout

Crossovers should be minimized as they add to the manufacturing cost. Flying lead crossovers (jumpers) are more costly and can create yield losses when there are a large number of wires in a hybrid package. Printed crossovers have an advantage in this situation in both yield and in crossover length. Therefore, if it appears that if a hybrid layout contains more than five flying lead crossovers, it should be converted to printed crossovers. If the total area of crossover insulation (dielectric) exceeds 50% of the substrate useable area, then crossovers should be replaced by another conductive layer using multilayer techniques and vias for layer interconnections.

Follow the rules established in Figure 5 for crossover designs. In general, all crossovers, flying or printed should be designed running parallel to the edges of the substrate. Crossover dielectrics will be designed to fit line to line with edge of first level conductors where interconnection is to be made. If the dielectric insulation is continuous under several conductors, crossover spacing may be reduced to .010 provided all other parameters are met. The optional step-down configuration of Figure 6 should be used in this case. This entails more preparation in the dielectric artwork but the rewards of higher circuit density are achieved. Use only single layer step-downs between adjacent conductive layers.

**CAUTION:** When designing printed crossovers on hybrids containing resistors, be sure that no resistor loops are formed by the printed crossover. If a loop is formed, the flying lead crossover must remain.

# Multilayer Design and Layout

Thick film multilayer circuits are fabricated with multiple conductor layers separated by dielectric layers. Interconnection between the conductor layers is performed by leaving selected holes (vias) in the dielectric layers and then metallizing the holes (via fills) to form a relatively flat structure. Multilayering a complex circuit increases the component density with significantly fewer wire bonds than an equivalent single layer circuit. Resistor printing can be used with multilayer circuitry in most situations. Use as few conductor layers as possible - to reduce field loss due to shorts, open vias, and test time. A four conductor layer design is easily fabricated and up to six are available at MHD. Beyond this, give consideration to increasing the size of the layout or contact MHD for further review of the circuit.

The dimensional constraints for conductors, bonding pads and mounting pads are the same as for single layer circuits (Tables A and B, and Figures 1, 2, and 3) except that the minimum dimensions for bonding pads should not contain vias. Wire or ribbon connections shall not be performed on that portion of conductors directly over vias. The following requirements apply to the design of multilayer circuits:

- Keep the first conductor .015" minimum from the edge of the substrate when the minimum substrate dimensions are used. Each successive conductor layer should recede .005" minimum from the previous conductor layer. Each successive dielectric layer shall recede .005" from the previous dielectric layer but overlap the lower conductor by at least .0025". (See Figure 7.)

- For complex circuits with constraints on the substrate dimensions, there is an option to the layer setback procedure. This option uses a laser scribed substrate that is printed on the side opposite the scribe lines. The dielectric layers overlap the boundaries of the scribe lines, yet still maintain a setback configuration, and the conductors are contained within the dielectric. Borders are removed after substrate fabrication. This procedure is particularly useful where numerous layers force a small effective area for chip and wire attachment. The overall requirements for conductor topography are the same, but area is gained where conductor setbacks would normally occur. More area is also gained if layer registration marks are located outside of the scribe lines. Dimensional requirements for this option are given in Figure 8.

- Conductors should be predominantly parallel on each layer, but perpendicular on alternate layers. Avoid long conductor runs where one line is directly over another. Lines should generally cross at 90° and if parallel runs are required, the top conductor should be a minimum of 5 mils from the edge of an adjacent underlying conductor. See Figure 9.

- Via dimensional requirements should be in accordance with Table C and Figure 10.

- Vias should be staggered (or stepped) when connecting two or more layers of conductors. E.g. for .010 square inch vias, there should be a minimum of .005" between edges interconnecting vias. See Figure 10. Straight passage (i.e. stacked vias) between a maximum of four layers is permissible if vias and via fills are .015 square inches or greater.

- Wire bonding to vias is not recommended. Locate vias "outboard" of wire bond areas as much as possible. See Figure 10.

- In those situations where a via connects between an alternating layer (i.e., not to any conductor in the middle layer) include a via fill conductor in the middle conductor layer. This ensures a more reliable interconnection and maintains a greater degree of via flatness.

TABLE C
Via and Through-Hole Dimensional Requirements

| Via Size and Spacing | Minimum Dimension (Inch) | Nominal Dimension (Inch) | See Figure 10 |
|---|---|---|---|
| Via Size and Corresponding Via Fill | .008 | .012* | 1 |
| Via to Adjacent Via Spacing | .010 | .015 | 2 |
| Via to Adjacent Conductor Spacing | .008 | .010 | 3 |
| Via to Edge of Dielectric Spacing | .015 | None | 4 |
| Via to Edge of Substrate Spacing | .025 | None | 5 |
| Via to Via Spacing for Step Configuration | .005 | .010 | 6 |
| Via Hole Diameter (in ceramic) | .006 | .008 | |
| Via Hole Annulus (for vias in ceramic) | .005 | None | |

* Stack Configuration

# Wire Routing Layout Considerations

## Bonding Clearance

Component and package profiles must be considered for optimum location of interconnection sites to ensure ease of wire bonding. The layout must provide adequate spacing between the substrate bond pads and both devices and package features. Profiles of the wire bond tools and associated hardware used should be available and considered in the layout process. Assume the maximum component dimensions and add .002" to the device height. See Figure 11.

### Wire Type and Application

Several factors affect the type of wire selected for hybrid packages: available bonding equipment, component metallization, substrate and package metallization, current requirements and location of components. The following guidelines will aid in this choice.

There are three basic types of wire interconnections in a hybrid package as illustrated in Figure 12. The length of a wire bond is defined as the span length as shown in the figure. Length as well as current requirements are specified in Table D. Current in the table is defined as maximum rated current, i.e., continuous current for direct current or an RMS current (peak current divided by 1.414) for an alternating or pulsed current. The selection of the appropriate wire size should be determined once this requirement is established. Gold wire is preferred over aluminum wire due to its versatility in hybrid interconnection. Aluminum wire should not be bonded to thick film gold unless compatibility has been previously established. Compatible thick film materials are listed in these guidelines. One mil and two mil wire are the typical wire sizes. The following lists wire sizes and their typical application in the hybrid:

| Wire Diameter (Mils) | Application |
|---|---|
| 0.7 | Die Pads .003 Square or Smaller |
| 1.0 to 1.5 | Chip to Substrate |
| 2.0 to 20 | Substrate to Substrate<br>Substrate to Package<br>Power (High Current) Chips to Substrate |

## Wire Routing

The depiction of a wire interconnection (bonding diagram) should be such that it clearly illustrates and defines the wire and the two terminating points. Thus, all wires can be shown as straight lines with a black dot at both ends. The following guidelines and the accompanying figures help form the wire routing requirements:

- Wires should be terminated at the center of a bond pad feature.
- Wires should be routed such that they do not obscure features, reference designations or symbols.
- Wires terminating on a long conductor run should be bonded at a point on the conductor that is closest to the respective component bond pad.
- Wire interconnections are preferably oriented in the X or Y direction. The preferred deviation from an X or Y axis when exiting from an IC chip is 30°. The maximum allowed deviation should be 45°.
- A wire should not be terminated on a via. There should be a minimum of .010" x .015" pad adjacent to the via area.
- A wire should not be routed across the face of a chip, another wire or a chip bond pad (functional or non-functional).
- A wire should not be routed directly from component or to a package lead bound pad - an intermediate termination point (bond pad) is required.
- For circuitry of any line width and space, the minimum distance separating any two wires (either at the termination or the span) should be .010" minimum, unless it is bonded to a common bonding pad. For common pads, the separation should be .005" minimum.
- Whenever a wire span is greater than 80% of its maximum length per Table D, an insulating layer should be placed over any unprotected underlying conductors. In this case, crossover dielectric should be used, except that the dielectric will fall short .005" from the substrate wire bonding pad.

## RESISTOR DESIGN AND LAYOUT

Thick film resistor materials are available in standard sheet resistances in a 1, 3, 10 progression from 1Ω per square to 10 MegΩ per square; i.e., 10, 30, 100, 300, 1K, etc. For an individual hybrid design, the choice of inks is dependent on the best fit to the resistor range. If the numbered ink is not available, blending of available materials can be done to achieve intermediate sheet resistances. Because of tolerances on the nominal values of resistor pastes, blending is required.

In choosing resistor inks, consider the increasing difficulty of manufacturing as the number of resistor printings increases. Try to limit the maximum resistor inks per substrate to five. Exceptions can be made if resistors can be made larger. At times, it is possible to eliminate an ink by replacing with a few discrete chip resistors. This can be very economical in the preproduction phase; however, in quantity production, it may be more cost effective to print another ink. The decision to use discrete resistors is based on the number, value and tolerances of the resistors. The yield of the substrate can increase if chip resistors are used for critical values. Thus, the yield of the resistors may be separated from the yield of the substrate. However, with proper design, it is possible to make one layout that can accommodate both printed and chip configurations for a given resistor. First design the resistor size based on the ink, then find a chip resistor size that spans the gap. Differences can be accommodated by changing the printed resistor width (keeping aspect ratio the same) or by increasing the end termination pad size. The chip resistors can be specified on the drawing with a note that allows replacement with a screened resistor. This technique, or the exclusive use of chip resistors, can have an advantage in prototype circuits where changes in resistor values are anticipated or in short-term programs where there is little time for redesign and optimization. Resistor chips/arrays should be seriously considered whenever available areas are small.

### Resistor Configurations

There are four preferred resistor configurations; rectangular, top hat, block serpentine and ladder. The rectangular configuration is the most preferred because it easily yields resistors with one percent tolerances (except for 10 MegΩ material which requires more care in trimming). This configuration, however, is typically limited to six squares as printed.

For resistors requiring more than six squares, the top hat or block serpentine configuration should be considered. Both of these are typically used to reduce the number of resistor materials on a substrate and can make use of the better properties of lower sheet resistance material. Unlike rectangular resistors where the resistance is reached by reducing the width, the top hat and block serpentine resistors reach value by increasing the path length. Tolerances for these two configurations are limited to $\pm$ 5% although some variations of the top hat can achieve $\pm$ 1% tolerances.

Conductor materials can be used to form low-value resistors. The maximum practical resistance value for metal resistor is approximately 5 ohms due to the low sheet resistance of conductor materials. These resistors consist of a series of shorting bars between long, narrow parallel conductors (ladder networks). Details of this and other resistor configurations are given in the following sections.

Variable resistor, i.e., resistors which require dynamic trimming within a large range of values present unique situation in resistor design. There is no single method of design configuration for these types of resistors. Each application must be treated separately and analyzed for power, available area, resistance range and tolerance requirements. Some situations will be addressed with a single rectangular, top hat or serpentine configuration where the as-fired values are slightly lower than the low end of the range and the maximum trimmed value will be at the upper end of the range. Other situations may require a series of any of these which are shorted with conductor metallization or wire bond pads and then opened and trimmed as needed by the performance requirements of the unit.

**General Resistor Guidelines**

The following general guidelines, Table E and Figures 14a and 14b apply to all resistor configurations.

- Resistor probe pads should meet the minimum requirements specified in Table E.

- Closed resistor loops represent an unacceptable layout practice due to problems in trimming to value. The proper method for establishing closed loops is to design the circuit loop open and then close the loop by wire bonding at assembly. Bonding pads follow the requirement previously specified.

- Resistors should be designed to be printed directly on the substrate surface. In some special situations, the resistors can be printed on dielectric material (e.g. a multilayer application). This can be a safe procedure. The decision to place resistors on dielectric should be made in conjunction with MHD.

- Resistors in parallel should not to be used in thick film layouts. They present the same problems as resistor loops and should be handled the same way. Resistors in series may be used for special purposes (e.g., active trims and/or top hats for gross range and rectangular for close tolerance).

- Rectangular configurations must be used for resistors with small tolerances and/or ratios. Exception: A top hat or serpentine resistor may be used in conjunction with rectangular resistors if ratios are more important than absolute tolerance.

- If space allows, design the conductor terminations to provide additional space at the edges of the resistor. The purpose is to allow widening the resistors in a second-generation artwork without having to alter the conductors.

- Resistors should be located as far from the edge of the substrate as possible. The clearance between any resistor and the edge of the substrate should be .050 inch minimum. See Table E.

- Resistors with high power dissipation should be evenly distributed on the substrate and should be placed near the substrate edge. If resistors are screened on both sides of the substrate, high-wattage resistors should not be placed opposite each other.

- Orient all resistors in either the X or Y direction (parallel to the substrate edges) to facilitate trimming and to reduce the variability introduced during the screening operation. The preferred methods is to orient all terminations in the axis parallel to the direction of squeegee travel. This permits all resistors to be in the same (long) direction, especially for resistors of the same sheet resistance value.

- The variability in the as-fired value of a thick film resistor is affected by the absolute size of the resistor as well as by the screen printing process variables, e.g., substrate nonuniformities; screen mesh, emulsion and tension variations; screening machine drift and position of the resistor on the substrate. In general, this variability can be reduced by designing resistors as large as possible. This means avoiding the minimum dimensional constraints and designing for as high a power rating as the area permits.

- The maximum resistor size is limited by available substrate area, substrate characteristics and material cost. As the length of a resistor approaches .500", substrate camber and flatness become progressively more important. The minimum resistor size is limited by the required power dissipation and production capabilities. The minimum practical size is .025" x .025". The aspect ratio limits can vary between 1/3 and 6 for rectangular configurations. Aspect ratios for other configurations are as specified in the applicable design section.

- Minimum Dimension -
  When designing a particular resistor, it is important to establish the minimum allowable size for the resistor. Since space is usually at a premium, it is desirable to make the area (length and width) of the resistor as small as possible. However, one of two factors dictates the minimum allowable size of a particular resistor: the limitations of the manufacturing capability or the thermal requirement that the resistor be of sufficient size to dissipate the heat generated when he resistor is functioning. The larger of the two has priority. Limits established by MIL-STD-883 prohibit any resistor width from being trimmed to less than 5 mils for thick film For good yields in production quantities, a more conservative figure of 10 mils should be used.

- Wattage -
  The layout designer has a strong interest in using the minimum geometries for any integral resistors. However, the design unit must also support adequate power dissipation. The maximum allowable power density must be established (i.e., the maximum wattage per square inch). One hundred watts per square inch is used for the maximum allowable power density on alumina (Al2O3) substrates. However, if other substrate material is used, such as beryllia (BeO), you should change the wattage density parameter to 250 watts per square inch. The actual resistor wattage must be divided by the allowable wattage density in order to determine the minimum area (square inches) that the resistor must provide in order to dissipate the heat. Given the maximum power density of the material used, the allowable minimum width and length, the length-to-width aspect ratio range and a list of allowable inks can be determined.

  If the width needed for power is less than the trimming recommendation, then the larger width is used and the length will be increased to retain the same ratio to the new width as existed in the calculation. Increasing these two dimensions will, of course, increase the area to greater than minimum. This is not only acceptable, it is desirable.

- Temperature Coefficients -
  Temperature coefficients of resistance for thick film resistors are generally from 50 - 250 ppm/degree Centigrade. After being subjected to 150°C to 1,000 hours, thick film resistor values may vary from 0.5 - 3%. For some critical circuits, it is therefore beneficial to have the substrates aged in a thermal chamber before they get trimmed.

- Resistor on the Substrate-
  Resistors can be fabricated on a multilayer substrate. This is usually done on the surface of the substrate, in an area devoid of multiple layers.

  It is desirable to print the resistors after the multiple layers are printed in order to avoid changes to the resistor values caused by subsequent firing cycles. However, when the resistors are fabricated after the multiple layers, the resistor screen/squeegee must pass over the step created by the dielectric edge. Screening the resistor paste on such a stepped surface requires greater space between the resistor and any nearby step for good process control.

  Resistors "down-in-a-hole" can only be screened prior to the dielectric. Clearance dimensions should be specified and the resistor design must compensate for the changes in resistivity due to subsequent firings. Such compensation requires experimentation which MHD can provide.

  Integral resistors can also be printed directly on top of multiple layers. This requires special resistor paste designed to be compatible with dielectric material used for multilayer fabrication. If a resistor is to be laser trimmed, there should be no conductors directly below the area of trimming. There is a high probability that the laser energy will burn through to lower layers. However, while undesirable, it is possible to successfully fabricate and trim circuits with such conductors directly beneath the trimmed area.

There are several noteworthy resistor configurations known as "top hats" as seen in the examples. By using top hat configurations, larger aspect ratios can be achieved within less space. Top hats also provide the capability to trim the resistance over a wide range. This capability can allow one basic substrate configuration to be used in various applications requiring a wide range of resistor values.

TABLE E

Dimensional Constraints for Thick Film Resistors
YAG Laser Trimmed

| Resistor & Pad Sizes and Spacing | Minimum Dimension (Inch) | Nominal Dimension (Inch) | Maximum Dimension (Inch) | See Figure 14 |
|---|---|---|---|---|
| Resistor Length (L), Top Hat Configuration | 0.050 | None | 0.500 | 1 |
| Resistor Width (W), Top Hat Configuration | 0.010 | None | None | 2 |
| Hat Width (Wh), Top Hat Configuration | None | None | 0.500 | 3 |
| Hat Length (Lh), Top Hat Configuration | 0.025 | 2W+0.005 | None | 12 |
| Resistor-to-Resistor Spacing (Active Parts) Same Ink | 0.015 | 0.025 | None | 5 |
| Different Ink | 0.030 | 0.050 | None | |
| Different Ink, End to End | 0.010 | None | None | None |
| Resistor-to-Conductor Overlap (Length) | 0.0075 | 0.010 | None | 4 |
| Resistor Width | 0.025 | 0.035 | 0.500 | 7 |
| Resistor Length | 0.025 | 0.040 | 0.500 | 6 |
| Termination Clearance | 0.005 | 0.010 | None | 11 |
| Conductor Pad Length (Beyond Resistor) | 0.005 | 0.0075 | None | 8 |
| Resistor Overglaze Overlap (Sides Only) | 0.005 | 0.0075 | None | 9 |
| Resistor Probe Areas (If Different from End Terminators | 0.015 sq | 0.020 sq | None | 10 |
| Resistor to Edge of Substrate | 0.050 | None | None | None |

**Rectangular Resistor Design**
Terms and Definitions

The following terms are used in the design of thick film rectangular resistors:

| | |
|---|---|
| R | Resistor Value in ohms |
| Pd | Powder Density in watts per square inch |
| Pr | Maximum Power dissipation of Resistor in watts |
| L | Length of resistor in inches |
| W | Width of resistor in inches |
| SR | Sheet Resistance of resistor material in ohms per square |
| N | Number of squares (R/SR) |

Design Procedure

The size of a resistor is largely dependent on the sheet resistance of the material selected and the maximum power dissipation. All materials in the following calculation assume a derated power density of fifty (50) watts per square inch at a 50% maximum trim width allowance. The following steps are used in the design of rectangular resistors.

1. Tabulate all resistors by tentative resistor material paste sheet resistance.

2. Reduce the number of materials to a maximum of three. Determine which resistors will require a number of squares outside the limits of N; i.e., $.33 \leq N \leq 6$. Where possible, use a lower sheet resistance material and increase N.

3. Select the factor F to establish the untrimmed resistance value. The distribution of untrimmed resistance value is approximately ± 30% maximum. Untrimmed resistors must be designed so that they do not exceed the upper tolerance limit for the required resistor. The resistance value to be used for the untrimmed resistor is determined by the resistor tolerances and production capability, which is based on empirical studies of the particular qualified resistor system. Therefore, untrimmed resistors (i.e., resistors which will be trimmed to value) are designed to a certain percentage (F) of the desired nominal resistance. This factor is dependent on the value of N and is as follows for .040" minimum lengths:

| Factor F | Range of N |
|---|---|
| .90 | $.33 < N < 2$ |
| .85 | $2 \leq N < 3$ |
| .80 | $3 \leq N \leq 6$ |

4. For resistors with N less than one, determine the untrimmed resistor length first using equation (1). If the calculated length is less than .040" minimum, increase the length to at least .040".

(1) $$L = \sqrt{\frac{P_R \times F \times R}{.5 \times Pd \times SR}}$$

Once the length is determined, the untrimmed resistor width is calculated using equation.

(2) $$W = \frac{L \times SR}{F \times R}$$

Round W and L to the next largest .005" increment after calculating both.

5. For resistors with N greater than one, determine the untrimmed width first using equation. If the calculated width is less than .040", increase the width to at least .040".

(3) $$W = \sqrt{\frac{P_R \times SR}{.5 \times Pd \times F \times R}}$$

Then the length is calculated using equation.

(4) $$L = \frac{W \times F \times R}{SR}$$

Round W and L to the next largest .005" increment after calculating both.

6. Check the power dissipation rating assuming a 50% maximum trim allowance using equation as follows:

(5) $$P_R = \frac{Pd \times L \times W}{2}$$

This value should be at least equal to the maximum power dissipation of the resistor.

**Example of Design Procedure**

An example is provided to demonstrate the procedure:

Design is a 6000 ohm, ± 1%, 1/4 watt resistor. Three resistor materials are potentially usable for this resistor, 1000, 3000 and 10,000 ohms per square.

The material which will result in the minimum number of screening operations will normally be selected. When power levels are low and size reduction is of primary importance, the ink which will yield the smaller resistor is selected. Each alternative is acceptable as will be shown in the following example.

| | | Sheet Resistance (SR) Ohms per square | | |
|---|---|---|---|---|
| | | 1000 | 3000 | 10,000 |
| 1. | $P_R$ (watts) | .25 | .25 | .25 |
| | Pd (watts/square inch) | 50 | 50 | 50 |
| 2. | $N = \frac{R}{SR}$ | 6 | 2 | .6 |
| 3. | Factor, F | .80 | .85 | .90 |
| 4. | When N < 1, calculate L first | | | |
| | L (Inch) = $\sqrt{\frac{P_R \times F \times R}{.5 \times Pd \times SR}}$ | N/A | N/A | .073 |
| | W (Inch) = $\frac{L \times SR}{F \times R}$ | N/A | N/A | .135 |
| 5. | When N > 1, calculate W first | | | |
| | W (Inch) = $\sqrt{\frac{P_R \times SR}{.5 \times Pd \times F \times R}}$ | .046 | .077 | N/A |
| | L (Inch) = $\frac{W \times F \times R}{SR}$ | .221 | .131 | N/A |
| 6. | Resistor dimension, L x W (Inch) | .225 x .050 | .135 x .080 | .075 x .135 |
| 7. | Check power dissipation (Watts) | | | |
| | $P_R = \frac{Pd \times L \times W}{2}$ | .28 | .27 | .25 |

As can be seen, all three pastes will produce a resistor meeting the required power dissipation rating.

**Top Hat Resistors**

There are several resistor configurations known as “top hats” as seen in the examples. By using top hat configurations, larger aspect ratios can be achieved within less space. Top hats also provide the capability to trim the resistance over a wide range. This capability can allow one basic substrate configuration to be used in various applications requiring a wide range of resistor values.

# Capacitors

Thick Film Capacitors are made with screen printed dielectric layers requiring four or more successive depositions: one for the lower electrode, two for the insulating dielectric layer to provide double thickness and freedom from pinholes and one for the upper electrode.

To reduce dielectric leakage from the surface and to allow for misalignment, the lower (and larger) electrode must be completely covered by the dielectric layer. The upper plate must be smaller than the lower plate. Thus, as long as the upper electrode is always fully within the area of the lower electrode and the dielectric, it defines the area of the capacitor. Also, as long as the dielectric extends beyond both electrodes, it prevents misalignment that might cause a short circuit. To provide separation from adjacent components, allow a 0.010 of free space outside the most extended layer.

An overglaze is sometimes deposited over the whole unit to provide further protection of the surface. A wiring lead from the upper electrode will frequently overlap and make connection to other conductors printed on the lower level in the same screening with the lower electrode.

Two conductors that cross should be treated as a capacitor. Use a low k dielectric for the insulator between the crossing conductors to minimize such parasitic capacitance..

For the initial footprint calculation, assume that the capacitor is square. Later on the square can easily be changed to a rectangle or some other form that will be more suitable for the available space. It may even be convenient to combine a capacitor with a crossover between the same conductors, thus reducing the number of crossovers and minimizing their adverse effects. Two 0.020" crossing connectors usually represent a capacitance of 2pf ; two 0.010" conductors, 0.5-1pf.

Screenable dielectric materials are characterized by the capacitance density, D, per square inch of area, A, of the (smaller) electrode. The basic formula for total capacitance, C, becomes C = DA. A variety of screenable dielectric materials are available providing both high and low capacitance densities, D, of approximately 1600-2500pf/square inch low and 25,000-65,000pf/square inch high, the crossover dielectric provides 700-1500pf/square inch.

To determine the footprint area, F, for each capacitor (where practical), select the dielectric material for all the capacitors and the crossovers to minimize the number of screening and firing operations. Then determine the size of the square for each capacitor by finding the square root of the required capacitor area, A, in inches. Add 0.060" and square the total to obtain the area of the footprint. Since A=C/D, we obtain in square inches:

$$F = (0.060" + \sqrt{C/D})^2$$

$$F = C/D + 0.0036 + 0.120\sqrt{C/D}$$

Excluding the overglaze, four screen printed layers are required for capacitor or crossover: namely two conductor layers and a double dielectric layer. Then add all area to be screen printed to determine the total footprint area, as in the example shown in Table 8.

Table F
EXAMPLE OF FOOTPRINT CALCULATION FOR CAPACITORS

| Capacitor Number | Total Capacitance, (C) (pF) | | Dielectric Density, (D) (pf/sq. in.) | Capacitor Area, (C/D) (sq. in.) | $\sqrt{C/D}$ (in.) | 0.060 + $\sqrt{C/D}$ (sq. in.) | Footprint, (F) (sq. in.) |
|---|---|---|---|---|---|---|---|
| C1 | 10* | | 1,000* | 0.010 | 0.10 | 0.16 | 0.025 |
| C2 | 100 | 2,500 | 0.040 | 0.20 | 0.26 | 0.068 | |
| C3 | 2,000 | 65,000 | 0.031 | 0.18 | 0.24 | 0.058 | |
| C4 | 5,000 | 65,000 | 0.077 | 0.24 | 0.30 | 0.090 | |

Total Capacitance = 7110 pF

Total Active Area = 0.158 sq. in.

Total Footprint = 0.241 sq. in.

- Note: Small capacitances may be larger when measured due to parasitic effects of conductors and substrate.

A rough estimate of footprint area may be made without regard to overlap and free spacing from A=C/D. If this approximate area is more than the selected substrate area can provide, it id necessary to make design compromises between printed and add-on components to reduce the capacitor area before continuing to the more accurate calculations. For large capacitance values, multilayer chip capacitors are available that require much less area than printed capacitors of the same value.

Capacitor tolerances are normally $\pm$ 20-30%, depending upon the uniformity and control of inks, screening and firing. Because of the danger of creating shorts by sand or laser blasting of their edges, printed capacitors are not usually adjusted or trimmed, although capacitors have been adjusted successfully by carefully trimming the top electrode only. The main difference in the dielectric materials is the magnitude of the relative perpetuity or dielectric constant K. Typical values of K are air 1, plastic 2-20, glasses 4-40 and polycrystalline ceramic materials 6-10,000.

Fired thickness of a typical encapsulant dielectric with one printing is 0.5 mils which is optimum for continuous pinhole-free films that can be readily trimmed. Typical properties of capacitor and multilayer dielectrics follow.

## Typical Fired Capacitor Properties

| | | |
|---|---|---|
| Dielectric Constant | (1kHz, 25°C) | 500 |
| Fired Dielectric Thickness, mm | (Double Printed) | 50 |
| Capacitance Density, pF/cm2 | | 26,000 |
| Dissipation Factor % | (1kHz, 25°C) | <3 |
| Insulation Resistance,Ω | (100V, 25°C) | $>10^9$ |
| Breakdown Voltage, V | | >500 |

## Typical Fired Multilayer Properties

| | |
|---|---|
| Fired Thickness: | 40-45microns (1.6-1.8 mil) (2 fired layers, 200 mesh screen) |
| | 45-50microns (1.8-2.0 mil) (3 fired layers, 325 mesh screen) |
| Dielectric Constant (K): | 8-10 |
| Dissipation Factor: | 0.5% |
| Insulation Resistance: | $>10^{12}$ Ohms at 100VDC |
| Breakdown Voltage: | >400 VDC/25microns (1.0 mil) |

## CIRCUIT LAYOUT

To estimate the design constants prior to layout, the development engineer should systematically determine the total area required and the power that will have to be dissipated for each component on the thick film hybrid. For more detailed evaluation, the number of screen printings, number of devices and leads to be attached to the substrate and the number of attachment operations must also be determined. To simplify the evaluation prepare a design matrix such as that of Table G. Apply a combination of rule of thumb, standard equations and standard data to each component in turn.

Please contact MHD for any assistance on layout questions or problems.

# Preparation of Master Artwork

The preparation of the master artwork may be either positive or negative. In reverse order, if a black resistor on the substrate is considered a positive image, then the printing screen has a reverse pattern, or negative image. The screen in turn was produced from a positive image, consisting of a black emulsion on the top side of a clear sheet of film as the image is properly viewed (right-reading). The positive image was made from the original negative master artwork. Therefore, it is apparent that in preparing the artwork for thick film application, the required deposited layer must appear as a transparent image. This results in a light field (i.e., dark image) mask with the emulsion up for screen preparation.

# Orientation And Registration

## For Single Image

During the printing of thick film patterns it is necessary to locate the pattern on the substrate. Therefore, it is helpful to incorporate orientation marks on the artwork to position it on the substrate.

Artwork for thick film circuits generally contain three orientation marks positioned near the edge of the substrate. These marks correspond to the three point alignment system being incorporated on all substrate holding fixtures and are centered at each point of pin-to-substrate contact. The first layer of artwork should contain these marks in a position where they will always be visible - usually in the borders of waste edge (if used).

In addition to the orientation marks, registration marks for multiple layers are required. Each pattern should contain the registration marks which superimpose themselves when the conductors, dielectrics and resistors are in proper alignment.

The size and location of the orientation and registration marks can be determined by MHD.

## For Multiple Images Per Substrate (Step-and-Repeat)

For patterns with areas less than one square inch, (e.g., resistor arrays) consideration should be given to fabricating multiple patterns per substrate. This is commonly known as "step-and-repeat" process. The decision to use the step-and-repeat ("multiple-up") technique is based on economic and technical factors. The circuit designer must first analyze the technical requirements and advantages and weigh them against the economic factors. Sometimes the column and small size of the pattern necessitates going to a step-and-repeat pattern. Conversely, the high complexity or fine geometry may warrant going to a single image.

From an artwork standpoint, the orientation marks for single images per substrate do not apply. Instead, they will be replaced by “L” shaped alignment marks at the corners of the image. During the Step-and-repeat artwork process, these marks are used to register the images on the masks. These marks are used to align the images to the laser-scribed substrate and will remain in part of the pattern. If for some reason this is not desired, an alternate alignment mark is required outside if the pattern and will not appear on the step-and-repeat mask. Therefore, it cannot be used in alignment to the substrate. This alternate alignment mark consists of a horizontal center line. In all of these situations, the internal multiple layer registration marks will still apply to the step-and-repeat images. CAD techniques are required for cost effective multilayer construction. Micro-Hybrid Dimensions would be happy to assist in deciding in the quantity-up as well as with CAD design.

# Inspection

The standard thick film specification is MIL-STD-883D method 2032.1 . A copy of which follows.

MHD is also qualified as a supplier to its customer per:

- MIL-STD-45208A
- MIL-STD-Q9858A
- MIL-STD-38510H
- MIL-STD-105E
- MIL-STD-202F
- MIL-STD-209D

MHD's Clean room is certified Class 100,000 per Federal Standard 209-D.

**MIL-STD-883D**
**NOTICE 1**

* 3.1 Thin Film element Inspection. Section 3.1 pertains to Thin Film elements and has been deleted in this manual. Thick Film inspection resumes with section 3.2.